IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

LOW POWER DESIGN METHODOLOGY FOR ARITHMETIC CIRCUITS

B. Navya Sree*, Dr.M.Sailaja, K. Swetha Reddy
* M.Tech, Dept. of E.C.E, University College of Engineering, JNTUK, Kakinada. India- 533003.
Professor, Dept. of E.C.E., University College of Engineering, JNTUK, Kakinada, India-533003.
Member of Technical Staff, Seer Akademi, Hyderabad.

ABSTRACT

In this paper a modified Constant Delay Logic is been proposed to provide improved performance. Continues scaling in technology of VLSI circuits leads to increase in power consumption. Therefore designing a VLSI circuit technique with low power is a challenging task without sacrificing its performance. The Proposed logic is well suited for the critical path of a low voltage arithmetic circuits which consists of a large number of gates. The modified logic style is examined against the constant delay Logic and feed through logic, by analysis through simulation. A 8-bit ripple carry adder and 32 bit carry look ahead adder are been designed and their performance is evaluated using both proposed logic as well as existing logic designs. It is shown that the modified LP-HS Constant Delay Logic has better performance than that of the existing FTL and CDL logics. The simulations were done using HSPICE tool in 32nm, 45nm CMOS technologies with 1v, 1.1v supply voltages respectively.

KEYWORDS: Feed through Logic (FTL), Constant delay logic style (CDL), Low power and high speed CDL (LP-HS CDL), Power delay product (PDP), Energy delay product (EDP).

INTRODUCTION

IN recent years, power consumption reduction and increase in operating frequency of the CMOS integrated circuits without sacrificing the improvement in the performance is the topic of interest. Enhancement in the features from generation to generation can be observed because of the rapid growth in VLSI Technology. The different design levels, such as the circuit, layout and process technology level are been addressed because of the increase in low power very large scale integration (VLSI). At circuit design level, by implementing the circuit with a proper choice of logic style may give considerable saving in the potential of power.

According to the formula

$$P_{dyn} = V_{dd}^2 . f_{clk} . \sum_n \alpha_n . c_n + V_{dd} . \sum_n i_{sc_n} \quad \ldots\ldots (1)$$

The dynamic power dissipation depends on the voltage supplied to the circuit(V_{dd}), frequency of the clock signal applied(f_{clk}), short circuit power consumption (i_{sc_n}), switching activity of nodes (α_n) and capacitance of the nodes (c_n) where $'n'$ represents the number of nodes present in the circuit. Thus the requirements in choosing a logic style for the implementation of low power circuit must have reduction in the parameters like supply voltage, switching capacitance, switching activity and short circuit current. A logic style must be robust and have good electrical characteristics i.e., *decoupling* of inputs and outputs of gate along with the good *driving capability* and full *signal swing* at the outputs, so that in any circuit configuration the logic style may show the reliability in work and arbitrarily cascaded.

To improve the low power dissipation further a new logic family called Constant Delay Logic Style is been designed which has become a popular style in implementing complex logic circuits. In this paper a modified version of the Constant Delay Logic is been proposed to reduce power consumption and to achieve high speed performances. The proposed technique known as Low Power and High Speed Constant Delay Logic, results a superior performance in achieving reduced power dissipation and delay as a major concern. We attempt to address the short-comings of Feed through logic (FTL) and Constant Delay Logic (CDL). In order to prove the usefulness of the LP-HS Constant Delay

Logic, we have designed an 8-bit ripple carry adder (RCA) and 32 bit Wallace tree multiplier structures. To compare the performance of the proposed Logic with existing Logic designs, the parameters like power, power delay product and energy delay product are been calculated.

The rest of this paper is organized as follows: Section II reviews previous work on feed through logic (FTL) and explains the working of Constant Delay logic. Section III focuses on the design issues associated with Low power – High speed CDL. Section IV presents the performance analysis of both existing and proposed Logics using a buffer. The performance of an 8-bit ripple Carry adder (RCA) and 32-bit Carry Look ahead Adder structures given in section V, and Conclusions are derived in Section VI.

EVALUATION OF LP-HS CONSTANT DELAY LOGIC

Circuits having depth in the logic operation need to have better performance for which a new logic family called Feed through logic is proposed. However, this Logic exhibits many short-comings, including heavy power consumption, and reduced noise margin. To mitigate these problems, Constant delay Logic is introduced which shows robustness in its operation with minimized power dissipation, while maintain speed advantage of FTL. We demonstrate that, CD Logic has better efficiency and robust under extreme process and temperature variations.

Feed through Logic

The common practice of Feed through Logic is due to the need for faster circuits with low power consumption. It performs a partial evaluation of computational block before the input reach a valid level, and quick evaluation as soon as input arrived, which leads to high speed.

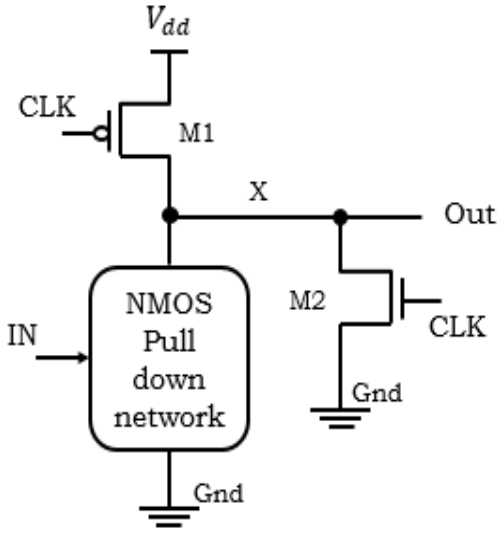


Fig 1: Schematic of Feed through logic

The basic schematic of feed through logic is shown in Fig 1. The working principle of FTL is as follows: when CLK is activated, the pre-discharge period begins and through M2 NMOS transistor, Out is pulled down to GND. When CLK is deactivated to Low, M1 (PMOS transistor) is on, M2 transistor is off, such that gate enters the evaluation period. If total inputs (IN) are raised to V_{dd}, Out enters the contention mode where M1 and transistors in the nMOS pull-down network (PDN) are conducting current simultaneously which allows the short circuit current. If PDN is off, then output quickly rises toV_{dd}.

Feed through logic is considered to be faster than traditional logic gates due to the following reasons:

- FTL has a reduced load as the logic expression requires only NMOS transistors
- Regardless of any logic expression, FTL have constant critical path with PMOS transistor.
- The pre-evaluation of output before the inputs from the preceding stage is ready. This feature results in very fast evaluation in computational block.

Despite of the advantage with FTL, it suffers from high short circuit current, and non-zero output voltage because of the contention between PMOS transistor and PDN. It is not practical to perform complex designs when multiple FTL stages are cascaded.

For example, consider a cascaded inverting circuit using multiple Feed through logics which is driven by same clock signal. This will result in false evaluation at the output of even numbered stages as the inputs to NMOS transistor are reset to zero during reset period which results no contention between PMOS and PDN transistors.

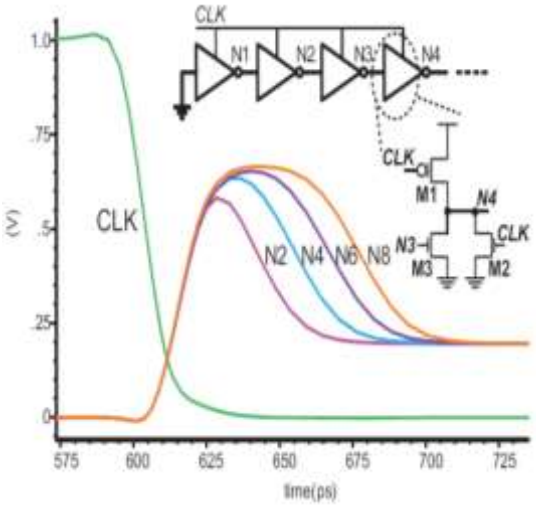


Fig 2: Result of cascaded Feed through logic

Constant Delay Logic Style

Regardless of the logic type any complicated design like adders can be designed using CDL because of its constant delay characteristic. The unique characteristic like the pre-evaluation of output leads to exhibit high performance over static and dynamic domino logic styles.

Constant Delay logic is proposed, to mitigate the problems with Feed through logic without sacrificing its feature of speed evaluation of output. The block diagram of CD logic is shown in Fig 3 which consists of *Timing Block (TB*), to create an adjustable window duration to reduce short circuit power consumption and a *Logic Block (LB)*, which helps in unwanted glitch reduction and making feasibility in cascading.

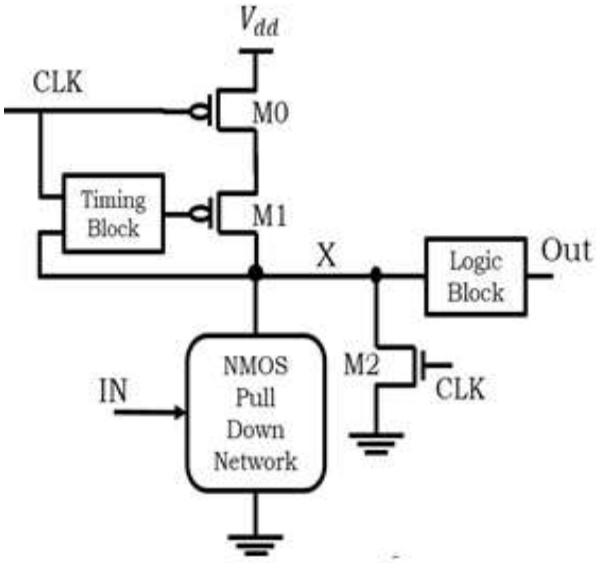


Fig 3: Block Diagram of Constant Delay Logic Style

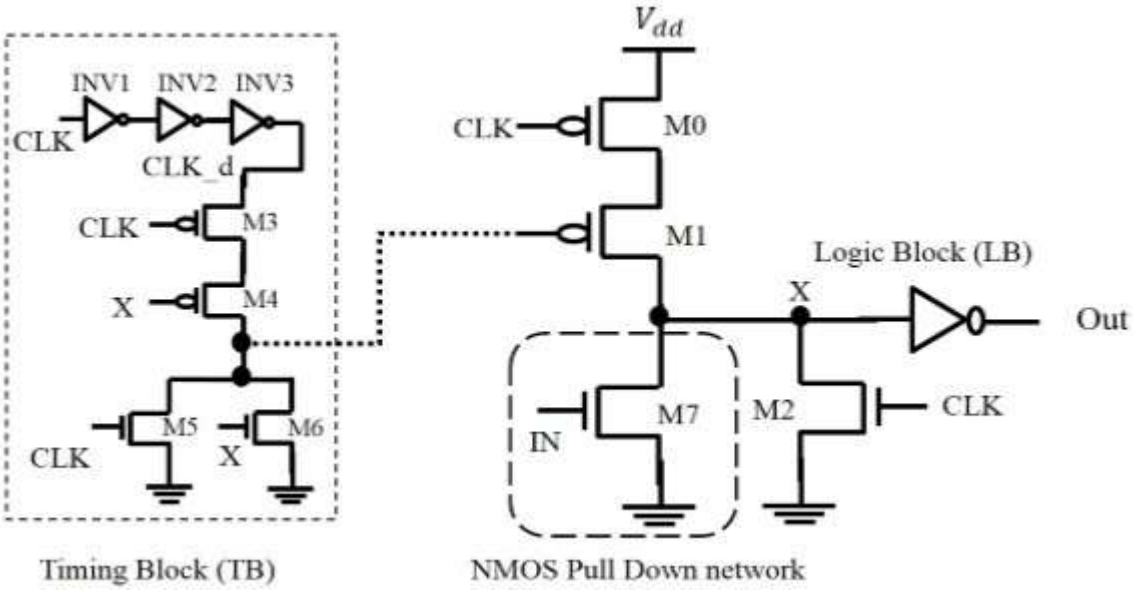


Fig 4: Schematic of a buffer using constant delay logic

The schematic of Buffer circuit using Constant Delay Logic which contain expanded diagram for timing block as well as Logic block is shown in Fig 4.The window duration is adjusted using the chain of inverters and self-resetting circuit is achieved by connecting the clock and intermediate node (X) as the inputs to NOR Gate. The inverter chain is used to provide a delayed clock so, the length of the inverter chain can be varied for certain delay depending upon the applied circuit. With the adjustment of window width, the period of contention mode can be reduced.

A simple static inverter is used as the logic in the case of dynamic domino logic. The above circuit consists only one NMOS transistor at pull down network as a buffer is to be designed.

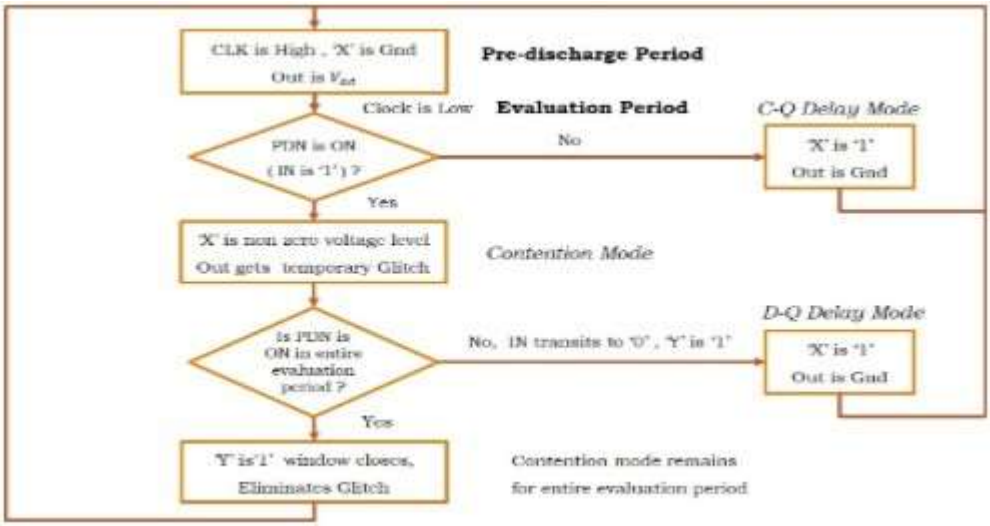


Fig 5: Flow chart of Constant delay logic operation

The flow chart in Fig 5 explains the working of constant delay Logic. The operation of the Constant delay logic can be explained in two modes.

i. Pre-discharge mode
ii. Evaluation mode

When clock signal activated, the logic is said to be in pre-discharge mode as the intermediate node (X) and Output are pre-discharged and pre-charged to Gnd and V_{dd} respectively. The logic is said to be in evaluation mode, when the clock signal is deactivated. Three conditions namely Contention, C-Q Delay and D-Q Delay takes place in Evaluation mode of the logic.

Contention Mode is achieved, when the input (IN) of pull down network (PDN) is at logic '1' then there exists a direct path between PMOS and PDN network which leads to the excess short circuit current flow, because of which the intermediate node (X) raises to non-zero voltage and output of the logic suffers from a temporary glitch.

C-Q delay i.e., delay from clock to output can be measured when IN transits to '0' before the transition of clock signal to '0', during this time 'X' raised to V_{dd} and output is discharged to ground.

D-Q delay mode happens when IN transits to '0' after the clock signal transits to Low, initially intermediate node 'X' enter to contention mode and raises to logic '1' later thus delay is measured from IN to Output.

Comparison between FTL and CDL

The Contention mode exists entire evaluation mode in FTL but the *Timing block* used in CD logic effectively reduces power consumption by shortening the duration of contention mode.

- The window duration can be customized depending on logic expressions to achieve minimal power dissipation without sacrificing the performance.
- Except in the contention mode, the internal node (X) is always connected to either V_{dd} or Gnd.
- CD Logic is suitable for high performance digital logics and shows better efficiency compared to other logic styles.
- It is shows its robustness even under extreme process and temperature variations.

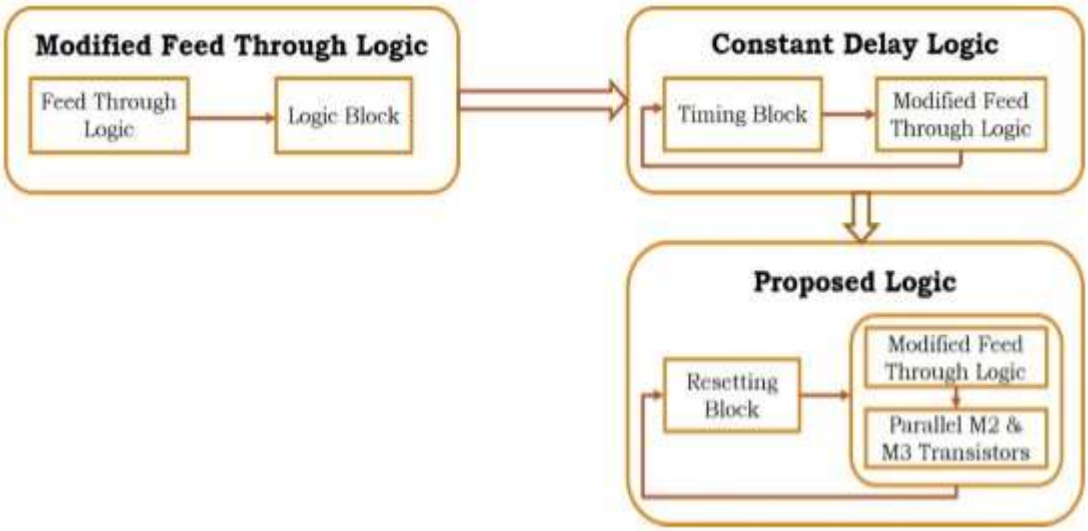


Fig 6: Chart specifying the flow of Logic Design

PROPOSED LP-HS LOGIC

The Low Power- High Power constant delay logic is been derived from the existing Constant Delay Logic. The proposed logic exhibits higher performance by reducing the power delay product. There are three major differences in the LP-HS logic when compared to existing logic.

- The window adjustment technique is eliminated in this logic.
- The evaluation transistor is altered as PMOS transistor instead of NMOS.
- M2 and M3 transistors are added below to pull down network to reduce power delay product.

The schematic of low power- high speed constant delay logic is been shown in Fig 7.

PMOS Transistors M0 and M1 whose gates are driven by the input clock signal and the output of resetting circuit respectively are connected in series. This combination helps in reducing power consumption as it increases the internal resistance. PMOS transistor M4 is acting as an evaluation transistor. The self-resetting logic which is a NOR gate is constituted by the transistors M5, M6, M7 and M8. This resetting circuit is driven by input clock signal and the output intermediate node 'X'. Input values 'IN' are given to the NMOS pull down network which is given according to the applied logic circuit. NMOS transistor M2 and a PMOS transistor M3 are connected in parallel helps to reduce the power delay product by placing them down to the NMOS pull down network The NMOS Transistor M2 is driven by the input clock signal and PMOS transistor M3 is at ground. Transistor M2 reduces the power consumption as it increases the dynamic resistance of the pull down network. The static inverter which is used to make the feasibility in cascading is figured using M9 and M10 transistors.

Operation of LP-HS Logic

The circuit works under two modes of operation.

- Pre-charge mode
- Evaluation mode

Pre-charge mode occurs when clock signal is deactivated and Evaluation mode happens when clock signal is activated. When clock signal is deactivated, PMOS transistor M4 gets ON which make internal node 'X' raise to high voltage and a low value at the output node.

When clock signal is activated, the transistor M2 gets ON, and gives the output according to the evaluated logic at the NMOS pull down network. During evaluation period, the transistor M0 which is driven by the clock signal is in OFF condition due to which the contention mode gets wiped out and thus window adjustment technique is eliminated in the proposed logic. One of the reasons for the power and delay reduction in the circuit is the due to the elimination of the window adjustment technique. The transistor M2 reduces the power consumption by providing the high internal resistance when it is in 'ON' condition. Transistor M3 an easy discharge of the value to the ground as it is always ON condition.

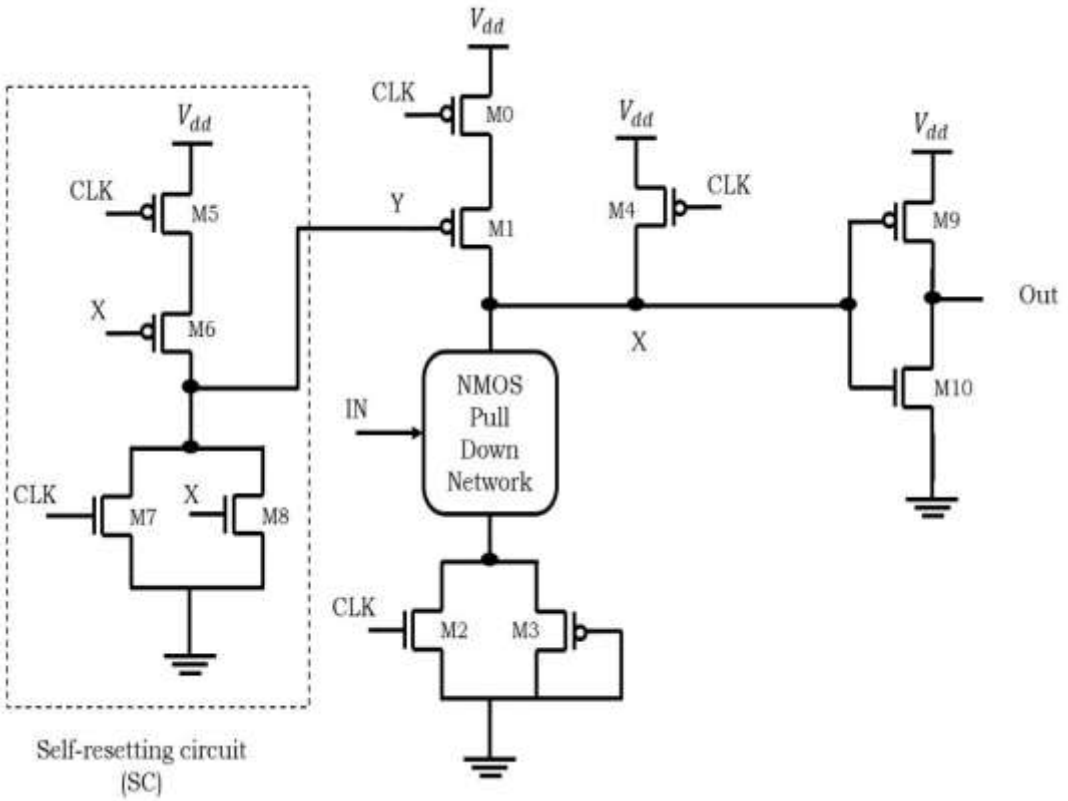


Fig 7: Schematic of LP-HS Constant Delay Logic

DESIGN CONSIDERATIONS OF PROPOSED LOGIC

Logic Sizing

The sizing of INV1 –INV3 and transistors used in timing block of CD logic and Self- resetting circuit (SC) are kept close to the minimum size so it doesn't take huge area. The length of these transistors can be altered which in turn provide a required window duration according to the applied logic.

Proposed logic is a rationed circuit which rely on the correct PMOS to NMOS strength ratio to perform logic operation. Basically PMOS strength ratio is often selected to be about one-third the strength of NMOS Pull down network. In LP-HS CD logic, intermediate node 'X' always connected to supply and ground thus it can be optimized for high to low transition. PMOS clock transistor can be sized larger than PDN to provide more speedup and maintain the output glitch at acceptable level.

The width of the PMOS transistor connected to clock signal is varied from 1µm to 3µm to check the change in the window duration of the logic.

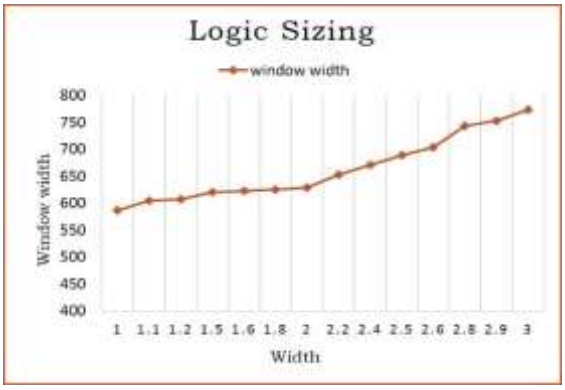


Fig 8: Graph showing variation of window width with transistor width.

Window width

The Window duration is a function of the logic expression, the number of preceding stages that are driving by the same phase clock signal, the maximum glitch level constraint, and the robustness of the overall system.

Moreover, as the window width prolongs, logic'0' noise margin improves margin improves while logic '1' noise margin degrades for both logic types. Such that, shortening the window duration not only reduces the power consumption but also improves the design overall robustness.

Power Consumption

The proposed logic's α is also 0.5, the power consumption is calculated only when is in the evaluation period. During this period, CD logic always dissipates power via either dynamic power dissipation (*X* goes to supply voltage and Out is discharged to GND) or short circuited current (contention mode). Even through this logic logic consumes more power, we believe that CD logic is still an attractive choice in a high-performance full-custom design as:

- The proposed logic is only intended to replace the critical path of the design.
- Power management techniques such as clock gating can be used where the clock connection to the module is turned off, this will significantly reduce dynamic power consumption of the logic

As the dynamic power depends on the supply voltage, frequency of clock which cannot be varied throughout the design. The load capacitance is varied from 2fF to 20fF to check the power consumption of the CD logic and the proposed logic.

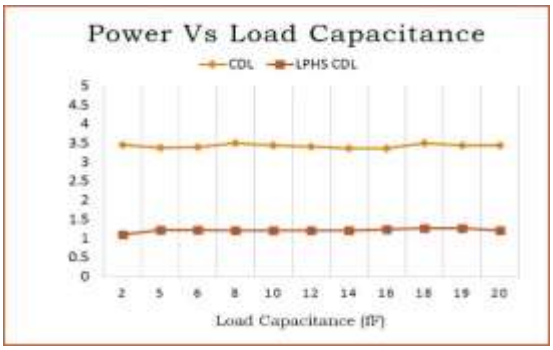


Fig 9: graph showing variation of Power with Capacitance.

Logic characterization

All simulation runs in this paper are done in schematic level (transistor netlists), in HSPICE simulation tool by Synopsis at 32nm and 45nm CMOS technologies with 1v and 1.1v supply voltages respectively

The power consumption calculation includes clock trees and data buffers, which are both sized to drive a fanout-of-4 (FO4) load. The outputs of all the logic gates are driving an identical 20 f F capacitive load. The window duration (width) is defined as the 50% point of the falling edge of input clock signal to the 50% point of the rising edge of output node of resetting circuit. The delay is measured at the 50% switching point of either the inputs to the 50% switching point of the output obtained.

In this section, all logic transistors have a 1-μm effective NMOS width. For this logic, the PMOS transistors' width is 2.8 μm. The transistor sizing are optimized primary for delay, because the main objective of this section is to explore performance advantage of proposed logic. The clock and data frequencies are set to 100 M Hz.

Logic performance using Buffer

Buffer logic is designed using FTL, CD logic and the proposed logic by replacing the pull down network with a NMOs transistor. The simulation results of the feed through logic, constant delay logic and the proposed logic are given in Fig 10, Fig11 and Fig 12.

Fig 10: Wave view of buffer using Feed through Logic

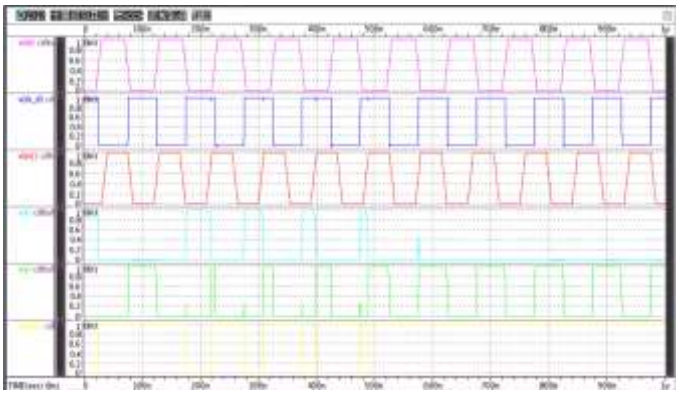


Fig 11: Wave view of buffer using Constant Delay Logic

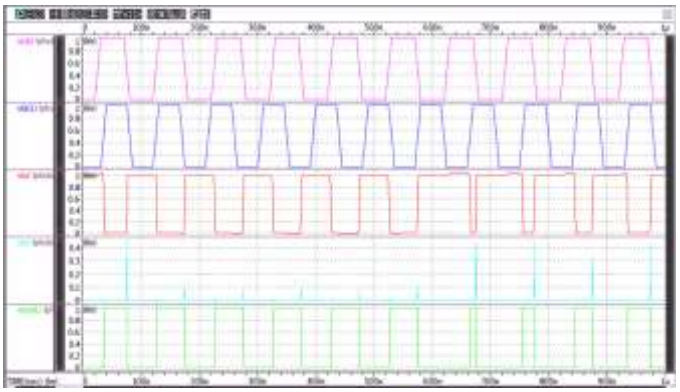


Fig 12: Wave view of buffer using Proposed Logic

It is observed from the Fig 10 that the feed through logic intermediate node goes to non-zero voltage level when the input transition occur i.e., in contention mode. Where as in constant delay logic the contention mode is reduced with the window duration, but the glitch at the non-zero glitch is seen at the intermediate node 'X' at the window width.

From the wave view of the proposed logic we can observe that the above problems associated with above problems are solved. The window duration is shortened to large extent so that the power consumption also reduced. The fluctuation in the intermediate node 'X' is due to the transition of input of NMOS from '0' to '1' after the pre-charge period is ended.

The tabular form specified in tables I and table II gives the comparison of power, delay, power delay product and energy delay product of logics in 32nm and 45nm CMOS technologies.

The proposed Logic exhibits the higher performance in the evaluation period and it is faster than other logics. This is contributed by:

- The pre-evaluation characteristic
- The logic is only placed in the critical path

Table I: Comparison of logics in 32nm technology

	FTL	**CDL**	**LPHS CDL**
Delay (ps)	2098.7	685.287	610.2
Power (uW)	94.7103	3.4215	1.080
Power delay product (fJ)	198.7704	2.3447	0.6591

Energy delay product (J. ps)	4.172 e-22	1.607e-24	4.022 e-25

Table II: Comparison of logics in 45nm technology

	FTL	**CDL**	**LPHS CDL**
Delay (ps)	2098.8	535.381	487.978
Power (uW)	105.417	5.2858	2.5687
Power delay product (fJ)	221.2465	2.8299	1.2535
Energy delay product (J.s)	4.643e-22	1.515 e-24	6.117 e-25

PERFORMANCE ANALYSIS

8 bit ripple Carry Adder

The simulation setup in this section is similar to that of logic characterization. Three 8-bit RCAs using FTL, CD logic style and proposed logic are simulated to compare their performances. The basic static full adder (FA) is implemented with 28 transistors with in favor of *C*out computation.

The main purpose of this 8-bit RCA is to demonstrate performance advantage of the proposed logic and to discuss the design considerations that should be taken into account when using this logic. Only the timing-critical carry generation is replaced with FTL, CD logic and proposed, while noncritical sum computation remains FTL in all three RCAs. The carry design of all tree logics and sum design are given in below figures.

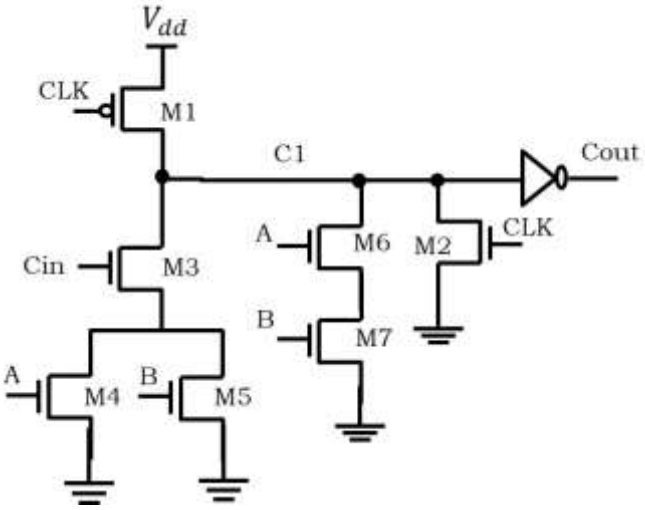


Fig13: Carry Generator using FTL Logic

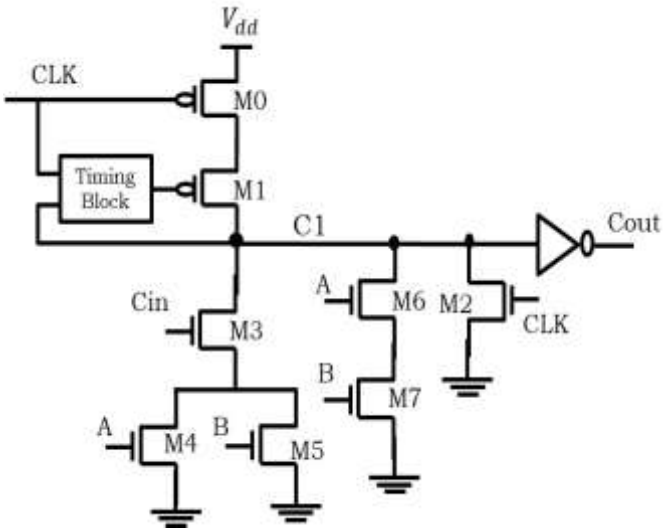


Fig14: Carry Generator using CDL Logic

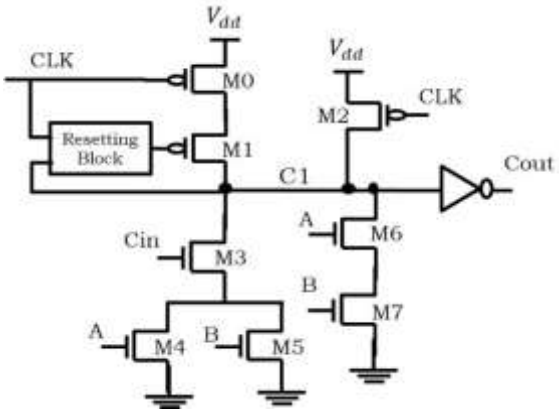


Fig 15: Carry Generator using proposed Logic

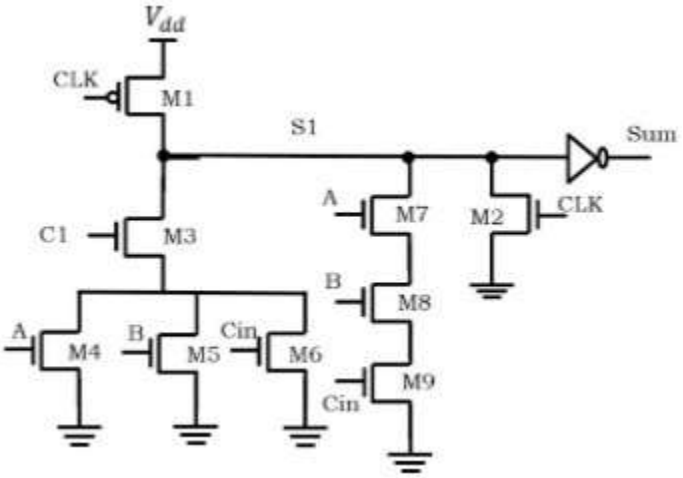


Fig 16: Sum Generator using FTL Logic

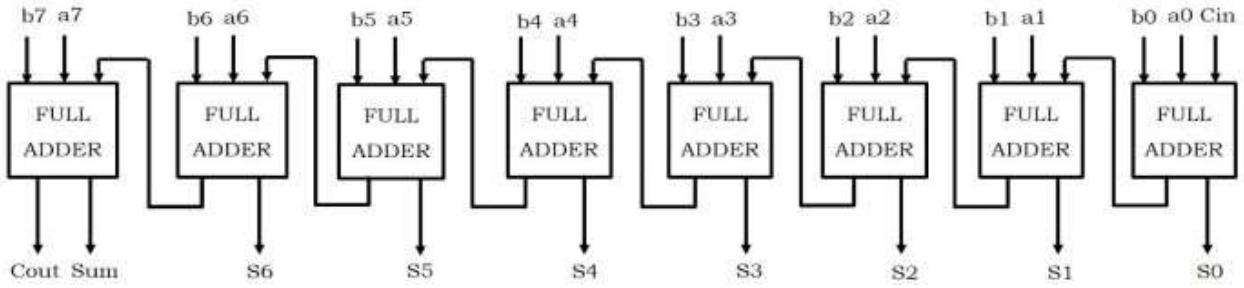
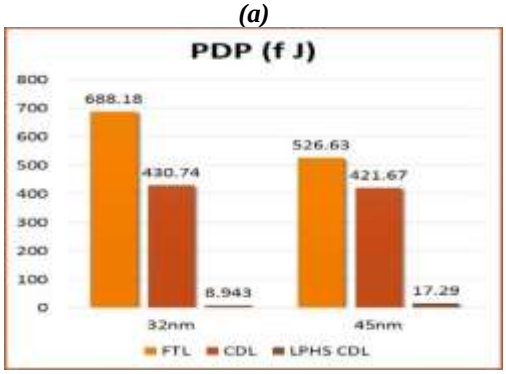


Fig 17: Schematic of 8 Bit Ripple Carry Adder

A Full-adder is made from three inputs 'A','B', 'Cin 'and two outputs Sum and a carry out. In 8 bit ripple carry adder 8 full adders are been cascaded to perform the design in which a0 to a7,b0 to b7, and Cin along with Clock signal are taken as inputs to the design and the outputs are Sum and Cout . In which Cout is obtained through the critical path. The comparative analysis of three logics are done between the input data to the Cout output signal.

The below given bar charts gives the comparative results of the three logics in power, power delay product and energy delay product.

(a)



(b)

(c)

Fig 18: Bar charts specifying Power, PDP and EDP values of 8-bit RCA

32 bit Carry Look ahead Adder

To analyze the performance of the proposed logic further a 32 bit carry look ahead adder is implemented. The detailed operations of CLA are described below and the schematic is displayed in Fig. 19. The 32-bit CLA uses eight 4-bit FAs with dedicated circuitry to facilitate carry generation. For the carry generation, only the critical path is replaced with different logic style. The maximum fan-in is limited to four, except in the case of proposed logic. In this case, the 4-bit critical carry generation path of CLA is

$G3{:}0 = G3 + P3\,(G2 + P2\,(G1 + P1\,(G0)))$ …… *(2)*

Where G denotes the generation which is the AND operation of inputs and P denotes the propagation which is the XOR operation of the inputs. These can be achieved by taking below given equations

$G1{:}0 = G1 + P1G0$, $P3{:}2 = P3P2$ …… …. *(3)*

Schematic of 32 bit carry look ahead adder is shown in below figure.

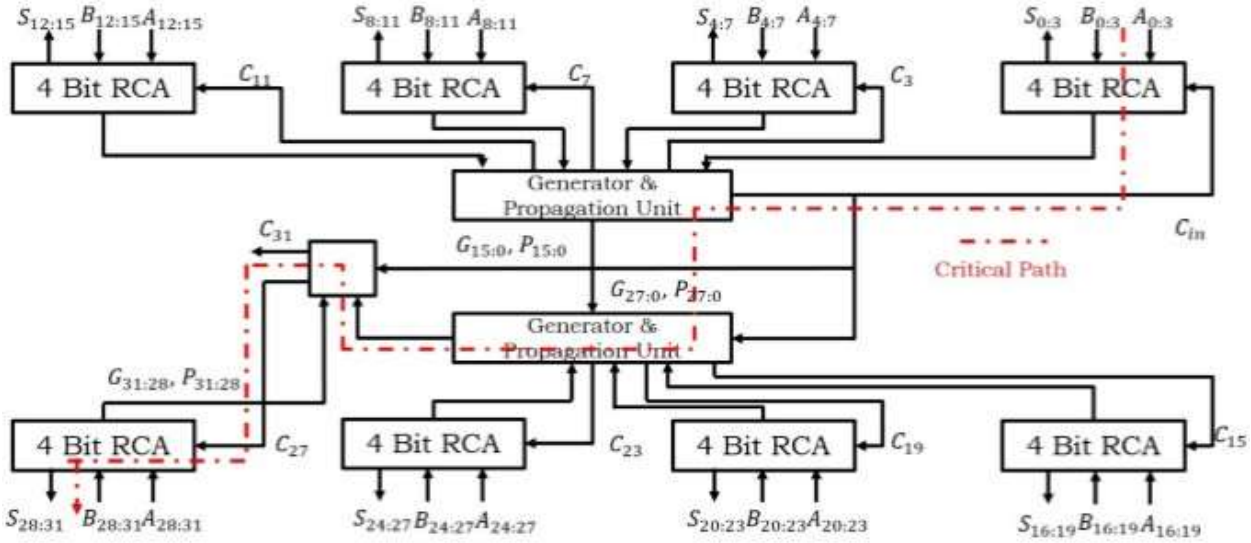
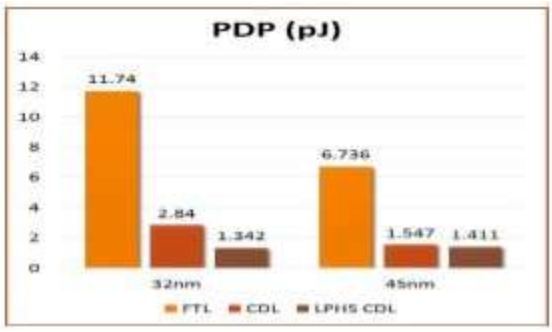
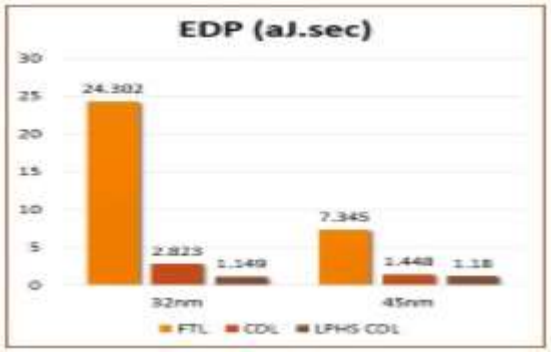


Fig 19: Schematic of 32 bit Carry look ahead adder

(a)



(b)



(c)

Fig 20: Bar charts specifying the Power, PDP and EDP values of 32-bit CLA

8-bit Wallace Tree Multiplier

Single–cycle two-phase 8-bit Wallace tree multipliers are implemented and analyzed. From first level to fourth level of Wallace tree utilizes the full adders and half adder in step by step process to produce partial products. During the last level final addition is carried out by an 11- bit carry bypass adder, as shown in the figure below. Only critical path of a final adder is implemented with various logic styles, while rest of the circuits remain in feed through logic. Simulation setups are similar to that of about applications.

The bar-charts given below summaries the performance results of 8-bit multiplier and the bar-charts illustrate the power, PDP and EDP of the different logic styles in 32nm and 45nm CMOS technologies. In 8-bit multipliers, as the various logics are used in the critical path only, the proposed logic has the lowest PDP and EDP values among all logic styles. in the adder Generator and propagate signals are not generated in this case, instead, direct inputs similar to 8-bit ripple carry adder are used to compute the carry.

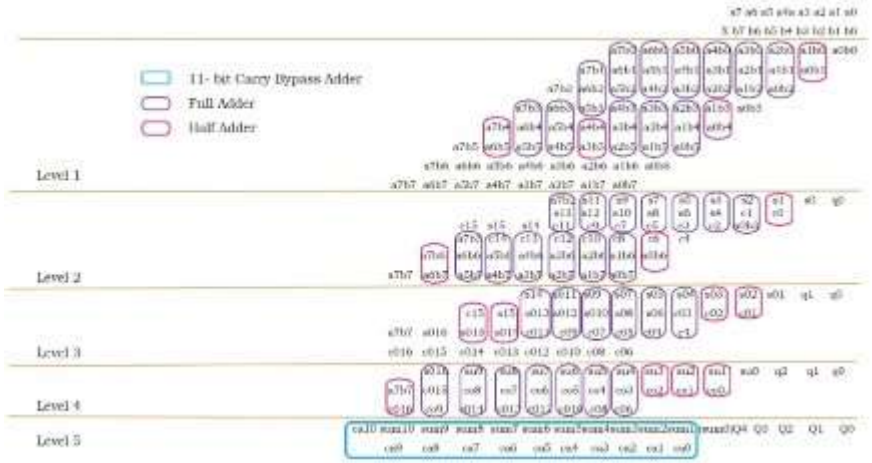


Fig 21: Schematic of Wallace tree multiplier

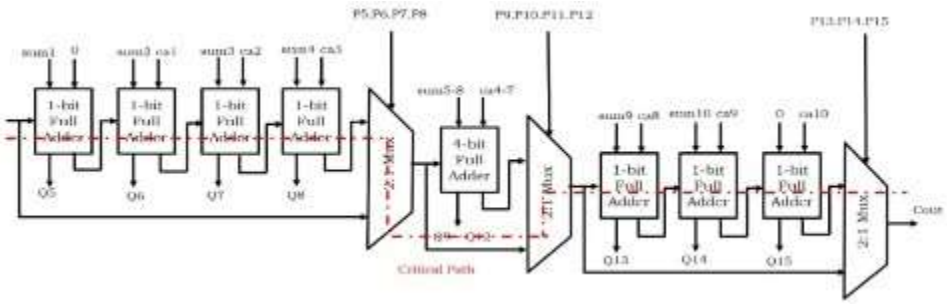
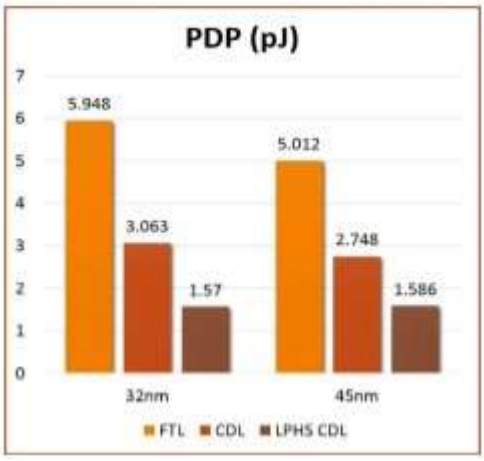
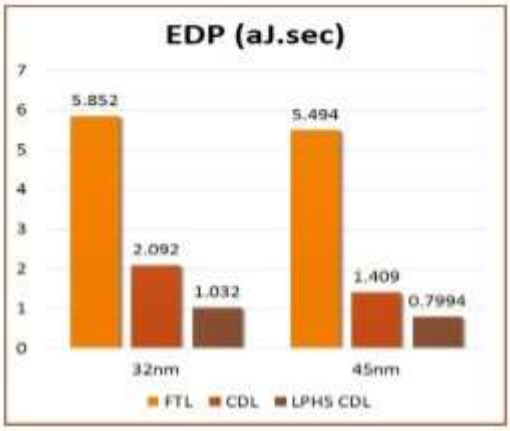


Fig 22: Schematic of 11- bit Carry bypass adder

(a)



(b)



(c)

Fig 23: Bar charts specifying the Power, PDP and EDP values of 8-bit WTM

CONCLUSION

In the era of high speed digital circuits CDL gives advantage of small power consumption compared to any other logics. In this paper, concept of constant delay logic (CD logic) and a modified version of CD logic termed Low Power High speed logic (LP-HS) is employed. The extension of Constant delay logic style to mitigate the problem with window adjustment and the addition of the transistors M2 and M3 in parallel below the pull down network used to reduce the power consumption in evaluation period. Modified LP-HS CDL also has lesser delay, reduced power consumption and improved PDP. Although it improves the performance of a circuit, it is achieved at a lesser number of transistors in reset block. The proposed circuit can be used for design of a low power designs where power consumption and high speed is of primary importance.

REFERENCES

[1] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.
[2] Chetana Nagendra, Robert Michael Owens and Mary Jane Irwin (1994)"Power-Delay Characteristics of CMOS Adders", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol.2, no.3, pp.377-381.
[3] Rajaneesh Sharma and Shekhar Verma (2011), "Comparitive Analysis of Static and Dynamic CMOS Logic Design", IEEE International Conference on Computing & Communication Technologies (ICACCT) pp.231-234.
[4] N. Goncalves and H. De Man, "NORA: A racefree dynamic CMOS technique for pipelined logic structures," IEEE J. Solid-State Circuits vol. 18, no. 3, pp. 261–266, Jun. 1983.
[5] C. Lee and E. Szeto, "Zipper CMOS," IEEE Circuits Syst. Mag., vol. 2, no. 3, pp. 10–16, May 1986.
[6] N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. Reading, MA: Addison Wesley, Mar. 2010.
[7] V. Navarro-Botello, J. A. Montiel-Nelson, and S. Nooshabadi, "Low power arithmetic circuit in feedthrough dyanmic CMOS logic," in Proc. IEEE Int. 49th Midw. Symp. Circuits Syst., Aug. 2006, pp. 709–712.
[8] V. Navarro-Botello, J. A. Montiel-Nelson, and S. Nooshabadi, "Analysis of high-performance fast feedthrough logic families in CMOS," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 6, pp. 489–493, Jun. 2007.
[9] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deepsubmicrometer cmos circuits," Proc. IEEE, vol. 91, no. 2, pp. 305–327, Feb. 2003.
[10] Sauvagya Ranjan Sahoo and Kamala Kanta Mahapatra (2012), ―An Improved Feedthrogh Logic for Low Power Design‖, 1st International Conference on Recent Advances in Information Technology (RAIT).
[11] Sauvagya Ranjan Sahoo and Kamala Kanta Mahapatra (2012), ―Performance Analysis Of Modified Feedthrough Logic For Low Power And High Speed‖ , IEEE International Conference on Advances in Engineering, Science and Management, pp.1-5.

[12] Sauvagya Ranjan Sahoo and Kamala Kanta Mahapatra (2012),―Design of Low Power and High Speed Ripple Carry Adder Using Modified Feedthrough Logic‖ , International Conference on Communications, Devices and Intelligent Systems (CODIS) pp.377-380.
[13] SRSahoo and K K Mahapatra, "An improved Feedthrough logic for low power circuit design" in 1st international conference on Recent Advances in Information Technology 2012, 713-716.
[14] Pierce Chuang, David Li, Manoj Sachdev (2013). “Constant Delay Logic Style”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems,vol.21, no.3, pp. 554-56.